REMARKS

Claim 1 has been amended to include the subject matter of claim 11 without intervening dependent claims. It basically goes to the concept of reducing pixel values to reduce circuitry needed to perform the sum of absolute difference determination, while at the same time getting the most bang for the pixel values used. Namely, by adding an offset to the reduced pixel values, one can move the pixel values into the dynamic range actually used by the reduced bit data.

It is suggested that somehow this occurs in the cited reference to Lin. However, all Lin ever does is use reduced pixel values. He never compensates for the reduced values by adding to those reduced values.

In the claimed invention, the number of bits is reduced and those bits have their values increased by adding an offset. All Lin does is reduce the number of bits, but he does not add an offset to those remaining bits.

For example, one way Lin reduces the number of bits is to cut off the least significant bits. Removing the least significant bits in and of itself does not add an offset, but, rather, subtracts from the full resolution or full length bit pixel values. Therefore, there is no basis to suggest that merely reducing the number of bits in the pixel would in any way inherently or otherwise increase the bit values of the bits within the pixel values.

Specifically, as explained in paragraph 37 of the present application, in order to make the data viewable within the limited dynamic range, which is the result of using reduced length pixel values, an offset is added to the data. Thus, in Figure 5A, you can see the effect that the data values are mostly in the upper part of the graph, while in 5B, they are mostly in the lower part of the graph. The view for SAD purposes is basically the upper part of the dynamic range and by adding offsets to the data derived from reduced pixel bit lengths, the data can be pushed into the portion of the dynamic range that remains available. Thus, the addition of a level offset compensates for the reduced bit precision without any significant cost in additional hardware.

On the same basis, reconsideration of the rejection of claim 26 is requested.

Respectfully submitted,

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